

# WELCOME

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## REVISION LOG

VERSION	EFFECTIVE DATE	DESCRIPTION OF CHANGE
001	2016 01	Module Creation and Release
002	2017 03	Format Update/Minor Type Corrections
002.1	2021 05	Formatting Updates - No Content Changes
002.2	2023 04	Inclusion of Measurement Standards for clarification, page iv. Minor appearance and format updates.
002.3	2023 06	Replaced duplicated Questions and Answers for Sub-Module 05, pages 5.9 and 5.10.

### MODULE EDITIONS AND UPDATES

ATB EASA Modules are in a constant state of review for quality, regulatory updates, and new technologies. This book's edition is given in the revision log above. Update notices will be available Online at [www.actechbooks.com/revisions.html](http://www.actechbooks.com/revisions.html)

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**Question: 5-1**

What is the difference between an inverter and a buffer?

**Question: 5-5**

Explain the logic function of the NOR gate.

**Question: 5-2**

Explain the logic function of the AND gate

**Question: 5-6**

What is the difference between an OR gate and an EXCLUSIVE OR gate

**Question: 5-3**

Explain the logic function of the OR gate.

**Question: 5-7**

What is the difference between the Negative OR and Negative AND gates and the NOR and NAND gates?

**Question: 5-4**

Explain the logic function of the NAND gate.

**Question: 5-8**

What is the difference between TTL (transistor-transistor logic) logic circuits and CMOS (complementary metal oxide semiconductor) logic circuits?

## ANSWERS

### *Answer: 5-1*

An inverter, also known as a NOT gate, inverts the input signal. In other words, if there was voltage at the input to the gate, there would be no output voltage. A buffer is a gate with the same output as the input used to isolate or amplify a signal.

### *Answer: 5-2*

For an AND gate to have a Logic 1 output, all inputs have to be Logic 1. In an actual electronic circuit, this means that for a voltage to be present at the output, the AND gate circuit has to receive voltage at all of its inputs.

### *Answer: 5-3*

In an OR gate, only one of the inputs needs to be Logic 1 for there to be an output of Logic 1. When both inputs are Logic 1, the OR gate has a Logic 1 output because it still meets the condition of one of the inputs being Logic 1.

### *Answer: 5-4*

The NAND gate is a combination of an AND gate and a NOT gate. This means that AND gate conditions must be met and then inverted. If a Logic 1 output is to exist from a NAND gate, inputs A and B must not both be Logic 1. Or, if a NAND gate has both inputs Logic 1, the output is Logic 0.

### *Answer: 5-5*

A NOR gate is an inverted OR gate. If there is to be a Logic 1 output, or output voltage, then neither input can be Logic 1 or have input voltage. This is the same as satisfying the OR gate conditions and then putting the output through a NOT gate.

### *Answer: 5-6*

An EXCLUSIVE OR (XOR) gate is the same as an OR gate, except for the condition where both inputs are Logic 1. In an OR gate, there would be a Logic 1 when both inputs are Logic 1. With an EXCLUSIVE OR gate, if both inputs are Logic 1, the Logic 1 output is excluded and results in Logic 0.

### *Answer: 5-7*

The output of a Negative AND gate is the same as a NOR gate, and the output of a Negative OR gate is the same as a NAND gate. However, the inputs are inverted in the Negative OR and Negative AND gates.

### *Answer: 5-8*

TTL bipolar junction transistor circuits operate with +5 volts power source. It uses positive logic, meaning Logic 1 occurs with +5 volts and Logic 0 is ground or 0 volts. CMOS logic circuits use less power and use fewer elements. CMOS transistor output is triggered by lower voltage and does not rely on current flow through the base-emitter junction. CMOS logic circuits are less susceptible to electrical interference and operate with a wider range of voltages (Logic 1 between +3 and +18 volts).